WHAT IS CLAIMED IS:

1. A crosspoint switch integrated circuit comprising:

an array of input ports;

an array of output ports;

a switch matrix configured to selectively connect said input ports to said output ports for conducting electrical signals therebetween; and

equalization circuitry coupled to at least partially offset transmission losses experienced by said electrical signal while external to said crosspoint switch integrated circuit.

2. The crosspoint switch integrated circuit of claim 1 wherein said equalization circuitry is configured to measure jitter within said electrical signals and to utilize jitter measurements as a basis for offsetting said transmission losses, said equalization circuitry being adaptive circuitry enabled to automatically select levels of equalization.

3. The crosspoint switch integrated circuit of claim 1 wherein said equalization circuitry includes a plurality of adjustable equalizers, said adjustable equalizers each having adjustable filtering characteristics within a fixed number of equalization settings.

4. The crosspoint switch integrated circuit of claim 3 wherein each said adjustable equalizer includes a plurality of switchable connections which individually adjust said filtering characteristics when activated.

5. The crosspoint switch integrated circuit of claim 4 wherein each said switchable connection includes a switch, at least some of said switchable connections including at least one component which significantly affects said filtering characteristics when said switchable connections are individually activated.

6. The crosspoint switch integrated circuit of claim 5 wherein at least some of said switchable connections are arranged in electrical parallel and said components include capacitors and resistors.

7. The crosspoint switch integrated circuit of claim 5 wherein at least some of said switchable connections are arranged in electrical parallel and said components include an inductor and a resistor.

8. The crosspoint switch integrated circuit of claim 5 wherein said switches are transistors and said components include at least some of resistors, capacitors, or inductors.

9. The crosspoint switch integrated circuit of claim 4 wherein adjustable equalizers are coupled to said input ports in one-to-one correspondence.

10. The crosspoint switch integrated circuit of claim 1 wherein said equalization circuitry is fixed with respect to providing levels of equalization to said electrical signals received at said input ports.

11. The crosspoint switch integrated circuit of claim 10 wherein said equalization circuitry includes a dedicated circuit for each said input port, said dedicated circuits being configured to provide one of a number of said levels of equalization, wherein said level of equalization of a specific said dedicated circuit is tailored on a basis of anticipated transmission loss for electrical signals received via the input port to which said dedicated circuit is dedicated.

12. A crosspoint switching arrangement comprising:

a plurality of input ports connected to channels having non-uniform frequency responses with respect to incoming signal transmissions;

a plurality of output ports connected to channels having non-uniform frequency responses with respect to outgoing signal transmissions;

a switch matrix enabled to dynamically reconfigure connections of said input ports to said output ports; and

equalization circuitry coupled to one of said input and output ports, said equalization circuits having filtering characteristics that are tailored on a basis of said frequency responses of said channels to which said specific ones of said input and output ports are connected.

13. The crosspoint switching arrangement of claim 12 wherein said equalization circuitry is an adaptive equalizer configured to automatically tailor said filtering characteristics.

14. The crosspoint switching arrangement of claim 12 further comprising memory configured to store equalization settings for said equalization circuitry, said equalization circuitry including a separate equalization circuit for each said channel for which equalization is to be applied, each said equalization circuit having adjustable said filtering characteristics within a fixed number of available configurations, said equalization settings stored at said memory including a selection of a particular available said configuration for each said equalization circuit.

15. The crosspoint switching arrangement of claim 14 wherein each said equalization circuit includes a default configuration of first connected circuit components and a plurality of alternative configurations, said default configuration achieving a first level of frequency-dependent compensation for effects of skin loss in signals conducted via said channels.

16. The crosspoint switching arrangement of claim 15 wherein each said alternative configuration introduces second connected circuit components to achieve different levels of frequency-dependent compensation for said effects of skin loss.

17. The crosspoint switching arrangement of claim 16 wherein said second connected circuit components are coupled to switches that selectively introduce said second connected circuit components, said switches being manipulated based upon said equalization settings stored in said memory.

18. The crosspoint switching arrangement of claim 17 wherein said equalization circuits are coupled to said input ports and are individually adjustable from an exterior of an integrated circuit chip package in which said equalization circuits and switch matrix reside.

19. A method of providing equalization for a crosspoint switch comprising:

determining signal characteristics related to signal transmissions via each of a plurality of ports of said crosspoint switch; and

setting equalization circuitry housed within said crosspoint switch such that each said port has filtering characteristics tailored on a basis of said signal characteristics for said signal transmissions via said each port.

20. The method of claim 19 wherein said step of setting includes selectively activating and deactivating switching devices which introduce parallel connections of resistances and capacitances within said adjustable equalization circuitry, said equalization circuitry being a plurality of adjustable equalization circuits.

21. The method of claim 19 wherein said step of setting includes selectively activating and deactivating switching devices which introduce series connections of resistances and inductances within said adjustable equalization circuits.

22. The method of claim 19 wherein said step of setting includes activating adaptive equalization circuitry.

23. The method of claim 19 wherein said step of setting includes entering equalization settings into an integrated circuit chip in which said equalization circuitry and a switch matrix reside.

24. The method of claim 19 wherein said step of determining said signal characteristics includes monitoring jitter at outputs of said crosspoint switch.